CLAIMS

1. A method for forming a multigate dielectric structure for a semiconductor device, said method comprising:

providing a substrate, the substrate having a surface with a first surface roughness;

providing a dielectric layer overlying the substrate and forming a dielectric/substrate interface between the dielectric layer and the substrate at the surface of the substrate, the dielectric layer having an initial thickness;

forming a patterned photoresist overlying the dielectric layer and the substrate, the patterned photoresist defining a region for formation of a gate dielectric of a desired target thickness;

etching the region so that a portion of the dielectric layer remains within the region, wherein the portion of remaining dielectric layer within the region has a first intermediate thickness, the first intermediate thickness being less than the initial thickness;

ashing the portion of remaining dielectric layer within the region, wherein ashing causes an increase in thickness of the dielectric layer remaining within the region from the first intermediate thickness to a second intermediate thickness;

cleaning the portion of the dielectric layer remaining within the region, wherein cleaning causes a decrease in thickness of the dielectric layer remaining within the region from the second intermediate thickness to a third intermediate thickness; and

thermally oxidizing the dielectric layer, wherein thermally oxidizing causes the portion of remaining dielectric layer within the region to have a desired target thickness, and further wherein the thermal oxidation increases a density of the portion of remaining dielectric layer.

2. The method of claim 1, wherein the substrate includes one of a bulk substrate and an SOI substrate.

3. The method of claim 1, wherein the dielectric layer includes a silicon dioxide layer.

4. The method of claim 1, wherein the region includes a high performance device region.

5. The method of claim 1, wherein the portion of the dielectric layer remaining within the region further prevents the dielectric/substrate interface from subsequently being breached by an etchant.

6. The method of claim 1, wherein the first intermediate thickness is on the order of less than ten (10) Angstroms.

7. The method of claim 1, wherein ashing further includes ashing the patterned photoresist for removing the patterned photoresist.

8. The method of claim 1, wherein the second intermediate thickness is on the order of eighteen (18) Angstroms.

9. The method of claim 1, wherein ashing includes exposing the portion of remaining dielectric layer to an oxygen plasma.

10. The method of claim 1, further comprising subsequent to ashing, performing a post-ashing clean.

11. The method of claim 10, wherein the post-ashing clean includes use of a sulfuric acid peroxide mixture (SPM).

12. The method of claim 1, wherein cleaning includes a preclean.

13. The method of claim 12, wherein a duration of the preclean is selected such that the preclean does not affect the first surface roughness of the substrate layer within the region.

14. The method of claim 12, wherein the preclean is maintained for a given duration without affecting a surface roughness of the dielectric/substrate interface.

15. The method of claim 12, wherein the preclean includes a piranha clean, followed by an ammonium peroxide mixture (APM) clean and a hydrochloric acid peroxide mixture (HPM) clean.

16. The method of claim 15, further wherein the APM clean is of a limited time duration, the limited time duration being determined as a function of a beginning thickness and a desired target ending thickness.

17. The method of claim 15, wherein the piranha clean includes use of a sulfuric acid peroxide mixture (SPM).

18. The method of claim 1, wherein the third intermediate thickness is in on the order of eleven (11) to fifteen (15) Angstroms.

19. The method of claim 1, wherein the dielectric layer includes a first thermal oxide, and wherein thermal oxidation of the dielectric layer forms a second thermal oxide at the dielectric/substrate interface, wherein the portion of the dielectric layer remaining within the region includes a composite of the first thermal oxide, a plasma oxide, and the second thermal oxide, and wherein thermal oxidation further densifies the first thermal oxide and the plasma oxide of the composite remaining within the region.

20. The method of claim 1, further wherein a surface roughness of the dielectric/substrate interface is substantially preserved.

21. The method of claim 20, wherein the substantially preserved dielectric/substrate surface roughness is a resultant surface roughness of the dielectric/substrate interface within the region that is substantially similar to the initial surface roughness of the dielectric/substrate interface.

22. The method of claim 1, wherein the portion of remaining dielectric layer is devoid of chemical oxide incorporation at the dielectric/substrate interface.

23. The method of claim 1, wherein the method includes one of a dual gate oxide (DGO) process and a triple gate oxide (TGO) process.

24. The method of claim 1, further comprising forming a semiconductor device structure using a portion of the portion of remaining dielectric layer within the region as a gate dielectric and forming another semiconductor device structure using a portion of the dielectric layer outside the region as a gate dielectric.

25. An integrated circuit having a multigate dielectric structure comprising:

a substrate, the substrate having a surface with a first surface roughness; and

a dielectric layer overlying the substrate, wherein the dielectric layer includes a first thermal oxide in first and second regions, wherein a dielectric/substrate interface is formed between the dielectric layer and the substrate at the surface of the substrate in the first and second regions, and wherein the dielectric layer in the first and second regions further includes a second thermal oxide at the dielectric/substrate interface, wherein a portion of the dielectric layer within the second region includes a composite of the first thermal oxide, a plasma oxide, and the second thermal oxide.

26. The integrated circuit of claim 25, wherein the portion of the dielectric layer in the second region is devoid of chemical oxide incorporation at the dielectric/substrate interface.

27. The integrated circuit of claim 25, wherein the integrated circuit includes one selected from the group consisting of a dual gate oxide (DGO) integrated circuit and a triple gate oxide (TGO) integrated circuit.

28. The integrated circuit of claim 25, further comprising a first semiconductor device structure formed in the first region using a portion dielectric layer within the first region as a gate dielectric and another semiconductor device structure formed in the second region using a portion of the dielectric layer within the second region as a gate dielectric.